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	INFORMATION DISCLOSURE CITATION BY APPLICANT *(USE SEVERAL SHEETS IF NECESSARY)*	APPLICANT: **Hidetoshi Narahara et al.**	
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U.S. PATENT DOCUMENTS

Examiner Initial		Document No.	Date	Name	Class	Subclass	Filing Date If Appropriate
KVdV	A	5,117,377	5/1992	Finman	703	2	
KVdV	B	5,479,440	12/1995	Esfahani	375	346	
	C						
	D						
	E						
	F						
	G						
	H						

FOREIGN PATENT DOCUMENTS

		Document No.	Date	Country	Class	Subclass	Translation
	I						
	J						
	K						
	L						
	M						

OTHER REFERENCES *(Including Author, Title, Date, Pertinent Pages, Etc.)*

KVdV	N	Analog Integrated Circuits and signal Processing, 14, pp. 113-129 (1997), di/dt Noise in CMOS Integrated Circuits, Patrik Larsson.
KVdV	O	EMI-Noise Analysis under ASIC Design Environment, Sachio Hayashi & Masaaki Yamada, DA Development Dept., Semiconductor DA & Test Engineering Center, Toshiba Corporation, pp. 16-21.
KVdV	P	IEEE Transactions on Components, Packaging, and Manufacturing Technology - Part B. Vol. 21, No. 3, August 1998, Interconnect and Circuit Modeling Techniques for Full-Chip Power Supply Noise Analysis, Howard H. Chen and J. Scott Neely, pp. 209-215.
KVdV	Q	Power Supply Noise Analysis Methodology for Deep-Submicron VLSI Chip Design, Howard H. Chen and David D. LingDAC97, Anaheim, California, (c)1997, pp. 1-6.

Examiner: KV Thang Jr	Date Considered 10/25/03

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